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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/809,646	03/16/2001	Shunpei Yamazaki	12732-021001 / US4802	5011

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EXAMINER	
DUONG, THOI V	

ART UNIT	PAPER NUMBER
2871	

DATE MAILED: 11/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/809,646	YAMAZAKI ET AL.	
	Examiner	Art Unit	
	Thoi V. Duong	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21 and 23-38* is/are pending in the application.

4a) Of the above claim(s) *10,12,14,16-21,23-25,29 and 31-35* is/are withdrawn from consideration.

5)☒ Claim(s) *3,6,9,11,13,15,28,30 and 38* is/are allowed.

6)☒ Claim(s) *1,2,4,5,7,8,26,27,36 and 37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/13/05 & 9/29/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on September 13, 2005 has been entered.

Accordingly, claims 1-3 were amended, claim 22 was cancelled, and new claims 36-38 were added. Currently, claims 1-21 and 23-38 are pending in this application; of these claims, claims 10, 12, 14, 16-21, 23-25, 29 and 31-35 are withdrawn from consideration and claims 1-9, 11, 13, 15, 26-28, 30 and 36-38 are considered in this office action.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 2, 4 and 5 are rejected under 35 U.S.C. 102(b) as being anticipated by JP 05-243262 (JP'262).

Re claim 1, as shown in Figs. 5 and 6, JP'262 discloses a semiconductor device comprising:

a substrate 11 having an insulating surface 13 (paragraphs 7 and 29);

a semiconductor layer formed over the substrate 11, said semiconductor layer having a channel forming region, an LDD region 29 and source and drain regions 31, 37, the channel region is between the LDD region;

a gate insulating film 13 formed on said semiconductor layer (paragraph 29);

a first gate electrode 15 comprising a first conductive film formed over said gate insulating film (paragraph 30);

a second gate electrode 17 comprising a second conductive film formed over said first gate electrode 15 (paragraphs 34 and 45),

wherein the width of said first conductive film in the longitudinal direction of said channel forming region is larger than that of said second conductive film (Fig. 6);

wherein said LDD region 29 entirely overlaps with said first conductive film with said gate insulating film 13 interposed therebetween and contacts said source and drain regions 31 (Fig. 6 and paragraphs 44-46).

Re claim 2, said channel forming region between the LDD region 29 overlaps with said second conductive film with said gate insulating film 13 interposed therebetween.

Re claims 4 and 5, as to the product-by-process limitation "the LDD region is formed in a self-aligning manner in accordance with the addition of an impurity element into said semiconductor layer with said second conductive film as a mask" of claims 4 and 5, it has been recognized that "Even through product-by-process claims are limited by and defined by the process, determination of patentability is based on the product

itself. The patentability of a product does not depend on its method of production. If the product in the product-by process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior art product was made by a different process". *In re Thorpe*, 227 USPQ 964,966 (Fed. Cir. 1985). See also MPEP 2113.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 7, 8, 26 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over JP 05-243262 (JP'262) in view of JP 6-148685 (JP'685).

The semiconductor device of JP'262 includes all that is recited in claims 7 and 8 except for said LDD region containing a region having a concentration of said impurity element gradient in a range from at least 1x10(17) to 1x10(18) atoms/cm3, while increasing as the distance from said channel forming region increasing.

JP'685 discloses an LDD structure manufactured by ion implantation wherein a concentration of impurity element gradient is 1x10(17) atoms/cm3 , while increasing as the distance from a channel forming region (below the gate structure) increasing so as to minimize a drain leakage current (paragraphs 20 and 25)

Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of JP'262 with the

teaching of JP'685 by forming an LDD region containing a region having a concentration of said impurity element gradient of at least 1x10(17) atoms/cm3 for minimizing the drain leakage current (paragraph 25).

Re claims 26 and 27, it would have been obvious to one having ordinary skill in the art that JP'262, which is a semiconductor device, is applicable to electronic equipment such as video camera, digital camera, projector, head mounted display, game apparatus, car navigation system, personal computer and portable information terminal for intended use.

6. Claims 36 and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over JP 05-243262 (JP'262) in view of Yamazaki et al. (Yamazaki, USPN 6,013,928).

The semiconductor device of JP'262 includes all that is recited in claims 36 and 37 except for an organic interlayer insulating film formed over the first and second gate electrodes.

As shown in Fig. 8F-2, Yamazaki discloses an insulating film 74 formed over a gate electrode 65, wherein the insulating film comprises an organic insulating material for planarizing (col. 9, lines 53-55).

Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of JP'262 with the teaching of Yamazaki to form an interlayer insulating film over the first and second gate electrodes, wherein the interlayer insulating film comprises an organic insulating material for planarizing (col. 9, lines 53-55).

Allowable Subject Matter

7. Claims 3, 6, 9, 11, 13, 15, 28, 30 and 38 are allowed.

The following is an examiner's statement of reasons for allowance.

Re claim 3, none of the prior art of record discloses, in combination with other limitations as claimed, an electronic equipment comprising: a first gate electrode comprising a first conductive film formed over the gate insulating film, said first conductive film having a tapered shape in cross section at an edge portion, wherein the gate insulating film has a first thickness in a region where the gate insulating film is covered by the first gate electrode and a second thickness in a region where the gate insulating film is not covered by the first gate electrode, and the second thickness is thinner than the first thickness.

The most relevant reference, USPN 6,462,802 B1 to Nishimura et al. (Nishimura) fails to disclose or suggest the gate insulating film having a first thickness in a region where the gate insulating film is covered by the first gate electrode and a second thickness in a region where the gate insulating film is not covered by the first gate electrode, and the second thickness is thinner than the first thickness. As shown in Fig. 1, Nishimura only discloses a first gate electrode 107 comprising a first conductive film formed over the gate insulating film 106 , said first conductive film having a tapered shape in cross section at an edge portion, wherein the gate insulating film 106 has an only thickness in a region where the gate insulating film is covered by the first gate electrode 107.

Re claim 11, none of the prior art of record discloses, in combination with other limitations as claimed, a liquid crystal display device comprising a pixel TFT and a driver circuit TFT, wherein the semiconductor layer of said pixel TFT comprises:

a channel forming region overlapping with said second conductive film with said gate insulating film interposed therebetween;

a first LDD region contacting said channel forming region and overlapping with said first conductive film with said gate insulating film interposed therebetween,

a second LDD region contacting said first LDD region, and

a source region and a drain region contacting said second LDD region.

The most relevant references, USPN 6,365,917 B1 to Yamakazi and USPN 6,369,410 B1 to Yamazaki et al., disclose the formation of the pixel TFT. However, these references are overcome by a statement of common ownership submitted by Applicant on June 14, 2004.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thoi V. Duong whose telephone number is (571) 272-

2292. The examiner can normally be reached on Monday-Friday from 8:30 am to 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Kim, can be reached at (571) 272-2293.

Thoi Duong

11/21/2005

ANDREW SCHECHTER
PRIMARY EXAMINER